PADERBORN UNIVERSITY

WiFi-based Human Sensing using FPGA-accelerated Lightweight Neural Networks (WiFiSense)
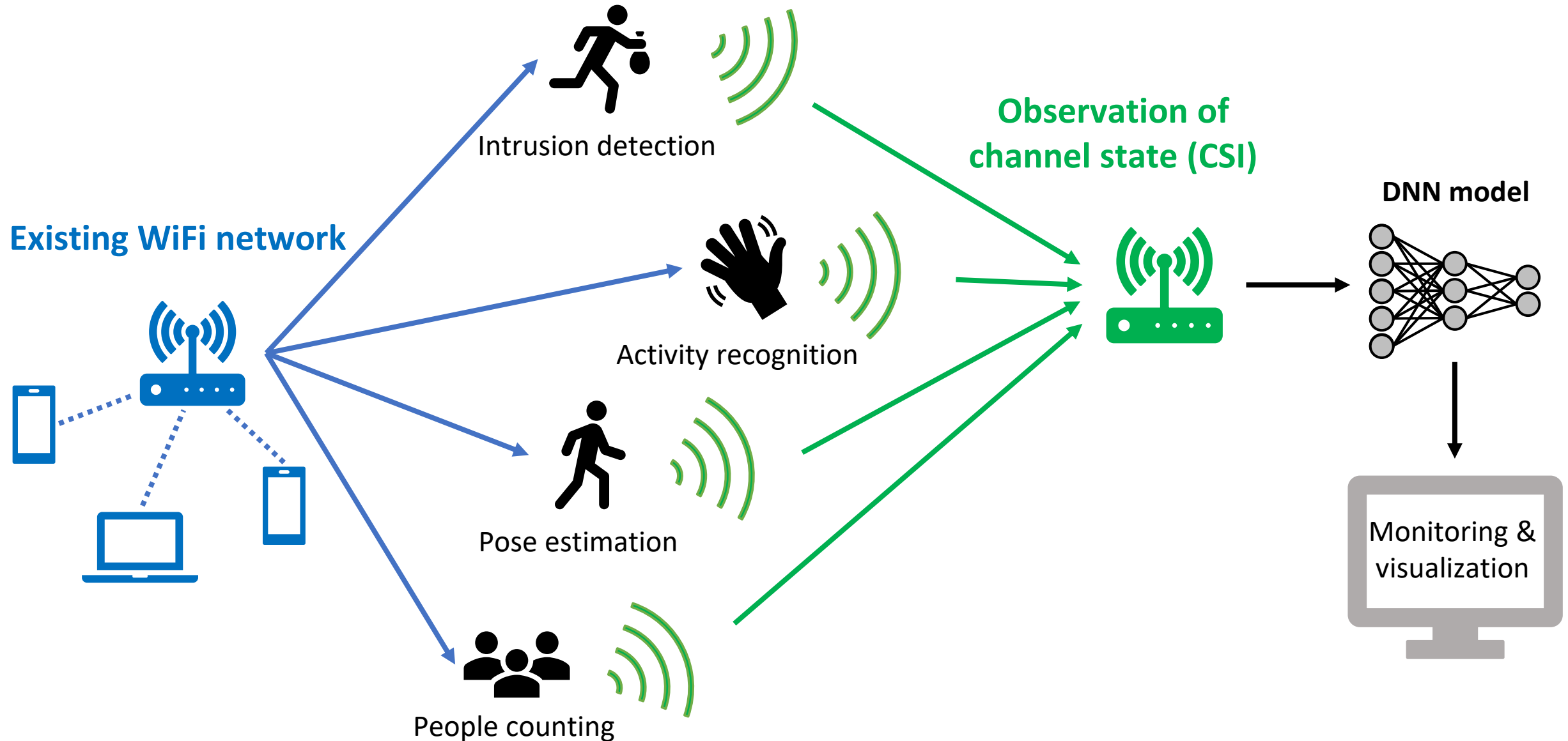
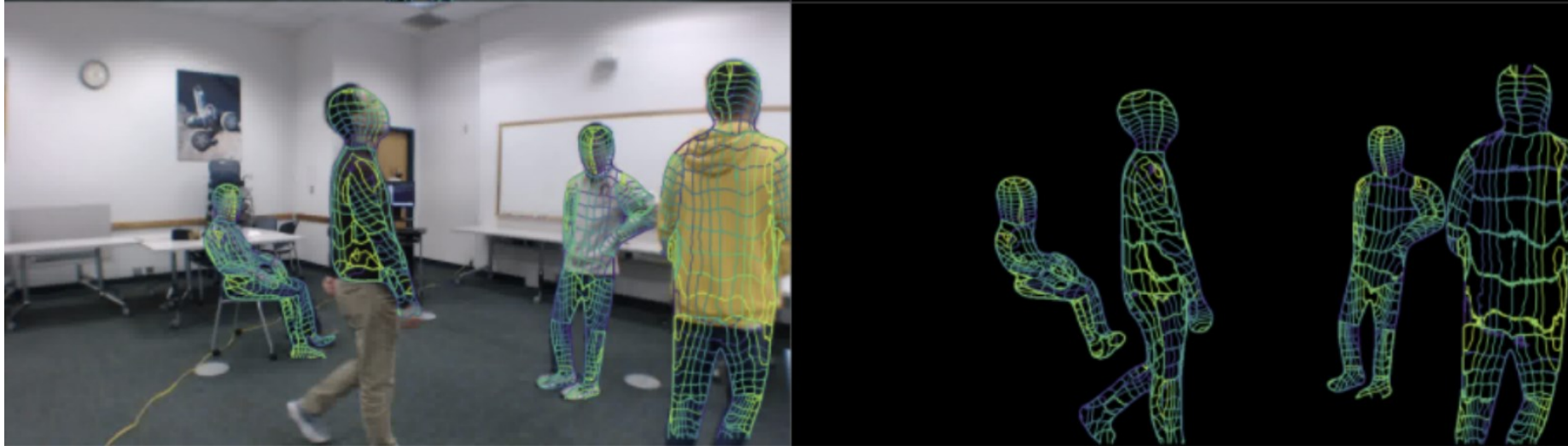## Project Group

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Computer Engineering Group, Prof. Dr. Marco Platzner

Application: Wireless Human Sensing

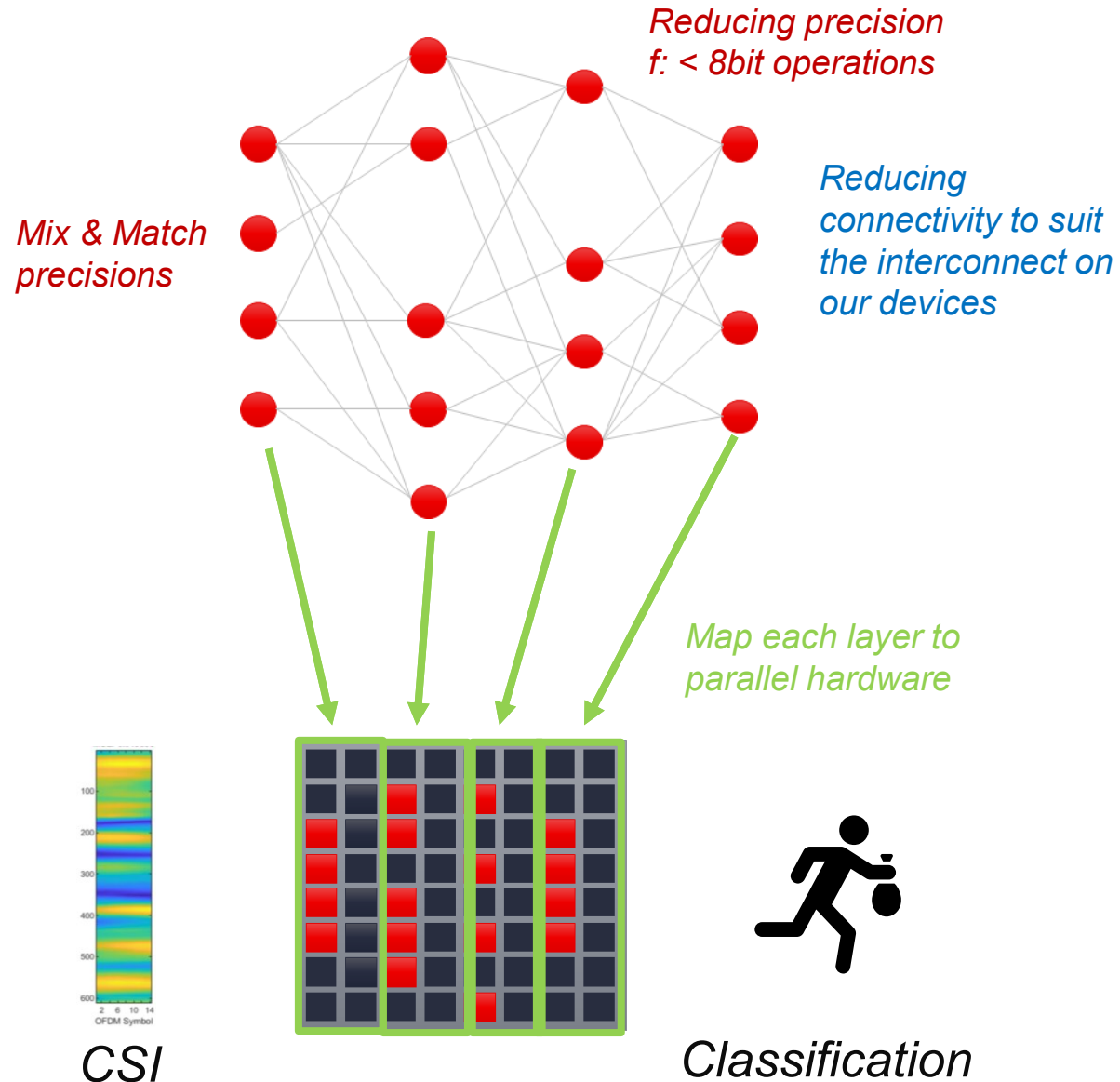- State-of-the-art example: "DensePose From WiFi" [1]:

Camera-based pose estimation   *WiFi-based pose estimation*

- Challenges for DNN inference at the edge
  - Real-time operation requires high throughput and low latency
  - DNNs require substantial compute & memory resources and continue to grow
  - Mobile, embedded devices are heavily power-constrained
- ➢ Novel solution: leverage custom FPGA acceleration for efficient co-design

[1]: Jiaqi Geng, Dong Huang, and Fernando de la Torre, "DensePose From WiFi". 2022, Available online at https://arxiv.org/pdf/2301.00250.

Reducing precision f: < 8bit operations

Mix & Match precisions

Reducing connectivity to suit the interconnect on our devices

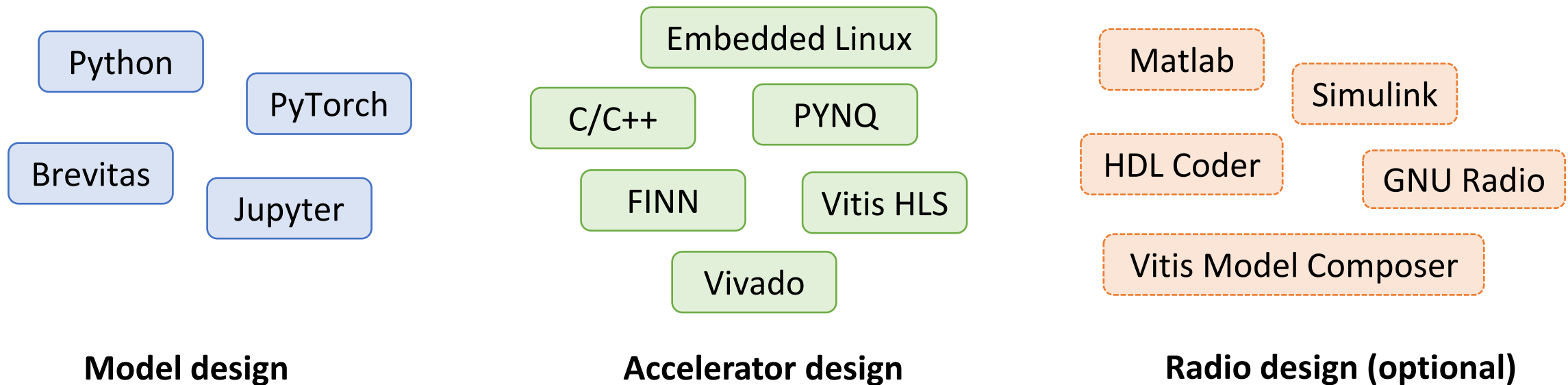*Map each layer to parallel hardware*

CSI

Classification

▸ Certain applications are feasible only through combined optimization of algorithm ***and*** hardware

▸ Research project (✓*FINN*): Generate custom-tailored DNN accelerators for FPGA

▸ FPGAs can scale DNN performance through extreme specialization

▸ **Reduced precision quantized arithmetic**
- **Arbitrary bitwidth, LUTs & DSPs**
- **Mix & match bitwidths between layers**

▸ **Fine-grained sparsity**

▸ **Scalable, layer-parallel streaming dataflow**
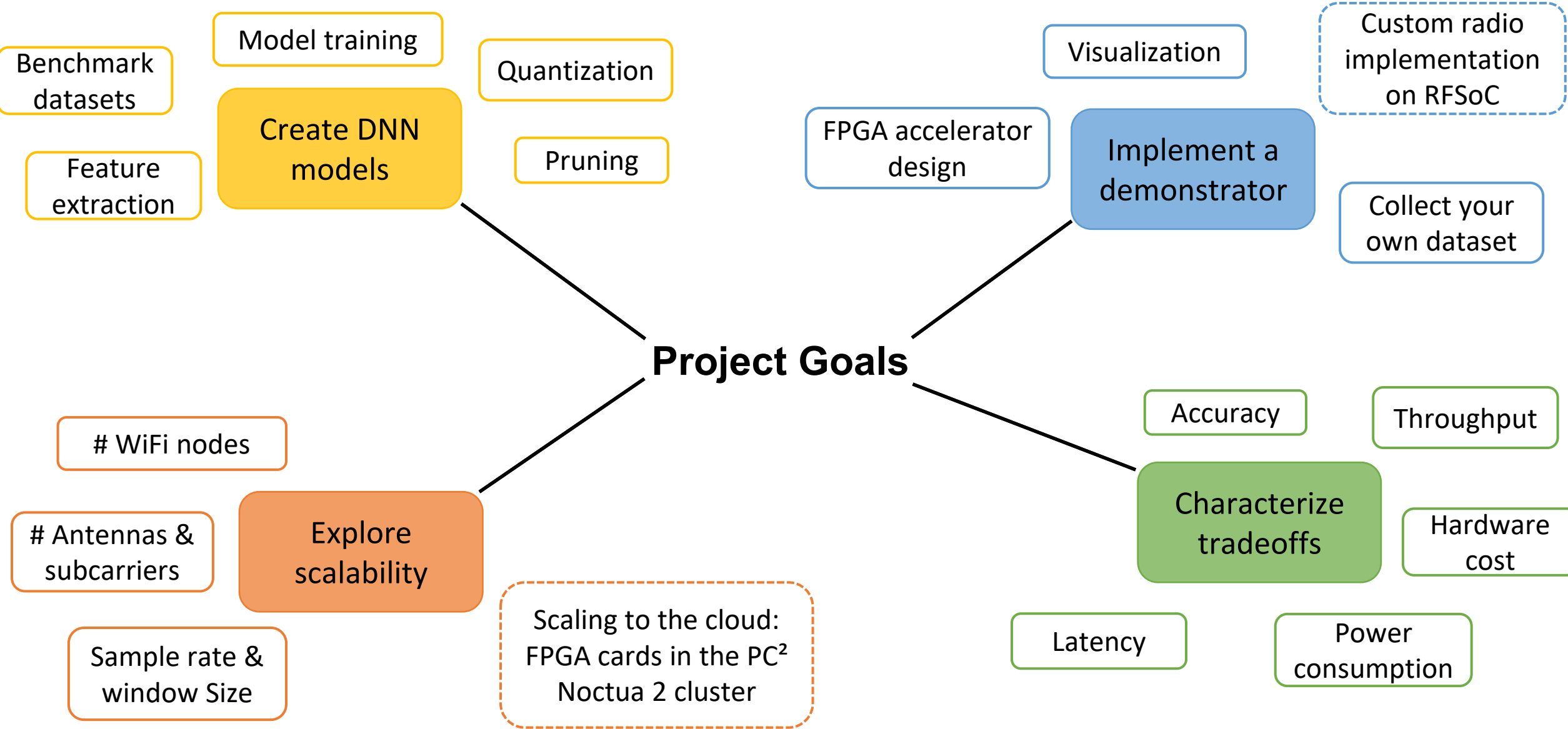
- Application process: Personal interviews
- You should bring knowledge or deep interest in at least one of these topics:
    - Machine learning, specifically deep learning
    - Signal processing or wireless communication networks
    - FPGA design
- Tools you will use:

Python	Embedded Linux	Matlab
PyTorch	C/C++ PYNQ	Simulink
Brevitas	FINN Vitis HLS	HDL Coder GNU Radio
Jupyter	Vivado	Vitis Model Composer
Model design	**Accelerator design**	**Radio design (optional)**

- Experience deep learning form an exciting new angle
  - Learn how to make DNN models lightweight (via quantization and pruning)
  - Co-design model and hardware accelerator using high-level FPGA compilers

- Build an end-to-end system
  - Learn how to analyze, pre-process, and extract features from datasets
  - Integrate sensor and accelerator components into a real-time system
  - Optional: Work with Simulink-based tools to design your own signal processing pipeline on RFSoC

- General skills
  - Team organization
  - Literature research
  - Experiment management

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Further information:
- Discussion right after this presentation
- Our website: https://en.cs.uni-paderborn.de/ceg/teaching/student-projects/project-groups/wifisense