High-Performance Computing Group
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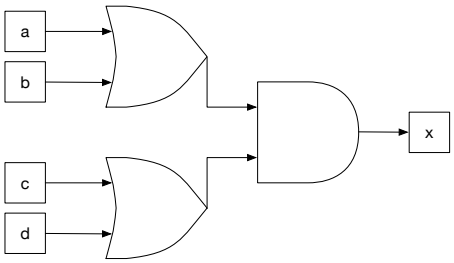
Analysis of Bit-level Operations on FPGAs

Bachelor Thesis

At a glance

- Research and model theoretical throughput of bit-level operations on FPGAs
- Investigate resource efficiency of building blocks with different specifications
- Integrate blocks into complete demonstrator design(s)
- Analyze practical limits and integration overhead

Several applications, most prominently from the bioinformatics domain, are performance limited by highly parallel and often specialized bit-level operations. FPGAs are an excellent hardware architecture for such operations, because each of their hundreds of thousands of lookup tables (LUTs) can be configured to perform any bit-level operations for one output bit given a few input bits. However, in practice it can be challenging to harness the full potential of the hardware when implementing such operations with high-level synthesis (HLS) tools. The goal of this thesis is to understand these limitations better and explore ways to overcome them.



a	b	c	d	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
…	…	…	…	…

```
bool x = (a || b) && (c || d);
```

In this thesis project, you will first research existing publications on theoretical potential and practically achieved results for bit-level operations on FPGAs. For a selected operations or combinations thereof, you will then investigate reported resource consumption values when implementing them with high-level synthesis (HLS) tools or exemplarily with hardware design languages (HDL). By integrating multiple different or identical blocks into a larger HLS-based demonstrator design, you will be able to analyze scalability challenges and resource overheads and explore best practices to overcome those.

Further reading:

- https://ieeexplore.ieee.org/abstract/document/9150362
- https://dl.acm.org/doi/10.1145/3597031.3597050

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