High-Performance Computing Group
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An Interactive Julia Interface for FPGAs

Bachelor/Master Thesis

At a glance

- Wrap the Xilinx Runtime (XRT) in Julia
- Increase the usability of the library by providing convenient abstraction layers
- Implement automatic detection of compute kernels and their input parameters on FPGA
- Evaluate final implementation with existing FPGA designs

The Julia programming language has gained increasing interest in scientific computing due to its simplicity and high performance. Still, currently there is no interface available to get fine-grained access to FPGA accelerator cards. Most often they only provide a high-level OpenCL interface which is not sufficient to inspect and interactively use compute kernels on the FPGA. This means, interaction with compute kernels on the FPGA often must be hand-written utilizing existing C/C++ libraries that provide the required functionalities or by using command line tools.

An interface that allows fine-grained interaction with the FPGA from the Julia REPL while also supporting the integration into high-performance scientific codes would bring FPGAs and Julia closer together.

- Focus on Xilinx FPGAs
- Wrap the C, C++, or Python Interface provided by XRT in Julia
- Implement kernel and input parameter detection to allow FPGA inspection from the REPL
- Automatic generation of kernel calls to improve usability

Further reading:
https://xilinx.github.io/XRT/master/html/

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