High-Performance Computing Group

Prof. Dr. Christian Plessl

Computer Science Department and

Paderborn Center for Parallel Computing

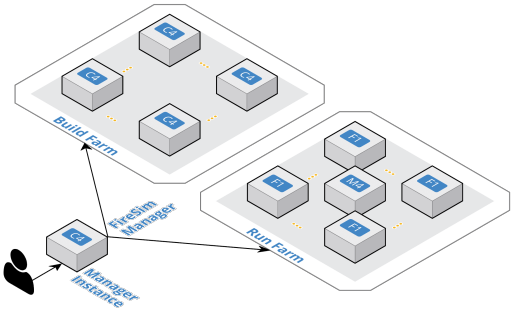
FireSim: FPGA-accelerated full-system hardware simulation

Bachelor/Master Thesis

At a glance

- Familiarize with SoC design accelerated with Chipyard/FireSim.
- Integrate FireSim into Noctua 2 cluster environment.
- Evaluate performance between Chipyard/Verilator and Chipyard/Firesim simulation.
- Evaluate performance between FPGA synthesis and Chipyard/Firesim simulation.
- Scale RISC-V multicore designs over multiple FPGAs.

The RISC-V instruction set is gaining importance in both research and industry. In the field of RISC-V System-on-Chip (SoC) design, there are robust open-source frameworks with software and hardware support available. Chipyard, for instance, combines SoC generators based on the Chisel HDL with simulation & synthesis tools. As designs grow in complexity, software-based simulations at the Register-Transfer Level (RTL) can become slow. To address this, hardware acceleration on FPGAs is becoming increasingly important, particularly for complex and interactive Linux workloads. FireSim stands out as a powerful open-source FPGA-accelerated simulator for full-system hardware designs.



FireSim has been prototypically demonstrated to work with the FPGA boards available in the supercomputer Noctua 2. However, a user-friendly integration into the supercomputer similar to the integration of the Amazon EC2 F1 FPGAs is missing. Furthermore, a systematic evaluation of the performance between software- and hardware-based simulation for a representative benchmark is still an open task.

Recommended skills:

- Interest in computer architecture design (RISC-V)
- Interest in modern hardware description languages (Chisel)
- Interest in software and hardware tool flow automation (Chipyard)
- Interest in hardware-acceleration (Noctua2)

Further information:

- Follow the links for further reading.
- Check this video for overall concept.

Contact:

Heinrich Riebler, Phone: 05251/60-5382 E-Mail: heinrich.riebler@uni-paderborn.de

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