High-Performance Computing Group
Dr. Tobias Kenter
Paderborn Center for Parallel Computing

Designing a RISC-V CPU in SUS

Master Thesis

At a glance

- Study the SUS Language
- Study the various architectures of CPU design (superscalar, out of order, etc)
- Implement a RISC-V design in SUS, evaluating multiple architectures

At PC2 we currently develop a new language and compiler, named “SUS”, that aims to help in the design and development of high-frequency FPGA accelerators. It does this by explicitly encoding pipelining information in the type of each wire, and using it both to automatically balance pipelines, as well as participating in type inference of submodule parameters.

SUS is designed for building FPGA accelerators, IE, structures that contain lots of free-flowing pipelines and a relatively small amount of state. A CPU is the polar opposite of this: Pipelines are short and rarely free-flowing. The internal state is plentiful and updates in complex ways. In a way, implementing a CPU in SUS would be the ultimate stress-test, and could reveal unexpected strengths or weaknesses.

Further reading:
https://github.com/pc2/sus-compiler
https://github.com/ultraembedded/riscv
https://csg.csail.mit.edu/6.375/6_375_2019_www/resources/riscv-spec.pdf

Contact:
Lennart Van Hirtum, Phone: 05251/60-4542 E-Mail: lennartv@mail.uni-paderborn.de

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