Tomasulo Simulator Web Application

• Motivation
  – teaching out-of-order execution simplified with simulator
  – existing simulators outdated (MIPS/DLX ISA)

• Tasks
  – develop browser-based RISC-V processor simulator that supports out-of-order execution
  – implement Tomasulo’s algorithm
  – visualize execution, dependencies, etc.
  – inspiration: http://nathantypanski.github.io/tomasulo-simulator/

• Required Knowledge
  – RISC-V instruction set (almost identical to MIPS)
  – out of order execution, low level software
  – simulation and interactive visualization with JavaScript

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