

Targeted Overclocking on FPGAs

Master Thesis

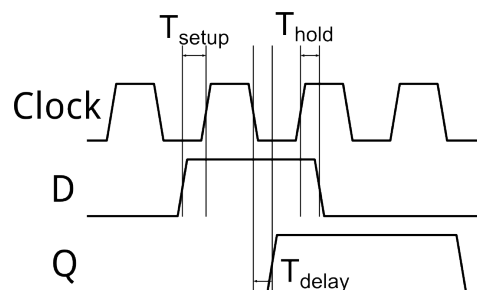
In a Nutshell



- Implement FPGA accelerator as a demonstrator
- Explore possibilities for overclocking of selected data paths in your accelerator design
- Evaluate error and unwanted side effects
- Explore dynamic overclocking at runtime

Raising the clock rate and increasing the number of transistors are no more feasible solutions to boost the performance of computing systems. Improving the speed and the energy efficiency of applications demands new approaches. Approximate Computing is a promising new paradigm, it trades in accuracy and reliability for efficiency [1].

Approximate Computing can be applied to different computing devices using various techniques. This thesis will focus on one specific technique: the overclocking of error-resilient data paths on an FPGA. Raising the clock rate above what is considered safe by the design tools has shown great potential for speedups [2]. However, only error-resilient paths must be overclocked to avoid undesired and unpredictable behavior.



In this thesis, the student will explore ways to apply targeted overclocking to an FPGA design. Nowadays, designing FPGA accelerators often involves high-level synthesis tools. The behavior of the designs generated by these tools is a particularly interesting topic to investigate. The student will evaluate the consequences of overclocking, characterize unwanted side effects and explore the possibilities for dynamic overclocking at runtime in order to minimize the errors.

Recommended Skills:

- Understanding of the fundamental functionality of digital circuits and their realization on FPGAs
- Desirable: Programming experience with FPGAs (HDL/HLS)

Initial Resources:

- [1] Mittal, S.: A Survey of Techniques for Approximate Computing
- [2] Shi, K.; Boland, D. & Constantinides, G. A.: Accuracy-Performance Tradeoffs on an FPGA through Overclocking

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